Docket #: S15-110

Symbolic Quick Error Detection (Symbolic QED)

During post-silicon validation and debug, manufactured integrated circuits (ICs) are tested in actual system environments to detect and fix design flaws (bugs). Existing techniques are costly due to ad hoc, manual methods. Such techniques become increasingly difficult to apply as ICs become increasingly complex. For example, traditional post-silicon validation and debug techniques may take days, weeks, even months of manual effort per bug.

Stanford and NYU researchers have addressed this challenge with a structured approach to post-silicon logic bug localization and debug. This technique is systematic and completely automated. As a result, this invention can significantly reduce the costs of post-silicon validation and debug. The technique can also be used to localize logic bugs during pre-silicon verification as well as emulation-based verification.

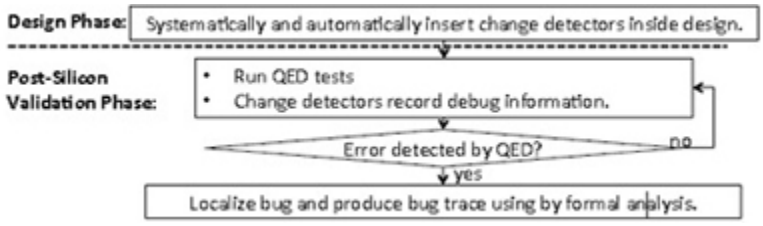


Figure: Overview of Symbolic QED

Stage of Research:

(as of Sept 2015)

- Proof-of-concept - validated on OpenSPARC T2 SoC (System-on-Chip), and has shown wide applicability to a variety of SoC designs from different companies.

Additional, complimentary QED Post-Silicon Validation technologies:

- Fast Quick Error Detection (Fast QED) Tests - **S13-388**
- Post-Silicon Validation for Complex SoCs with Accelerators - **S13-406**

Applications

- **System-on-Chips (SoCs)** - first technique to automatically localize logic bugs in SoCs during post-silicon validation and debug.

Advantages

- **Fully automated method** - unlike current manual techniques that can be extremely time consuming and expensive
- **Reduces cost and time** - requires only a few hours vs. other formal techniques which often take days or fail completely for large designs
- **Generates counterexamples (for activating and detecting logic bugs) that are up to 6 orders of magnitude shorter** than those produced by traditional techniques.
- **Effective for both bugs inside processor cores, bugs inside uncore components, as well as bugs related to power-management features.** Examples of uncore components include cache controllers, memory controllers, and interconnection network.

Publications

- "A Structured Approach to Post-Silicon Validation and Debug using Symbolic Quick Error Detection" by David Lin, Eshan Singh, Clark Barrett, and Subhasish Mitra. *In Proceedings of the 42^nd International Test Conference (ITC '15),* Oct. 2015. Anaheim, CA.

Patents

- Published Application: WO2016200723
- Published Application: 20180157574
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