Docket #: S16-244

Ultrathin, stackable, low power non-volatile memory for 3D integration

Engineers in Prof. H.-S. Philip Wong's laboratory have developed a lower power, three-dimensional resistive random access memory (RRAM) device using an atomically thin graphene edge electrode. RRAM is an emerging non-volatile memory technology with better endurance, retention and speed combined with lower programming voltages and higher device density than Flash memory. This invention improves the performance of RRAM by employing ultrathin graphene instead of traditional metal electrodes to assemble a stacked three-dimensional structure. The resulting memory provides extremely high storage potential in a small volume with low current, low power and low energy consumption. This bit-cost-effective 3D architecture could be a significant step towards a highly efficient, next generation computing system, particularly for mobile applications which require long battery life.

Stage of Research
The inventors assembled a resistive memory (~3 angstrom thick) stacked in a vertical three-dimensional structure and demonstrated some of the lowest power and energy consumption among the emerging non-volatile memories. They performed an experimental circuit analysis and demonstrated higher storage potential for these devices than for devices based on conventional electrode geometries.

Applications

- **Non-volatile memory** - three-dimensional resistive random access memory (RRAM) structures which could be:
    - a component of an integrated circuit, particularly for mobile applications that require long battery life
    - external data storage

Advantages

- **Ultra-thin structure:**
  - graphene monolayer electrode is ~3 angstroms (~20-30X thinner than conventional 3D vertical memory stack)
  - extremely dense architecture provides high storage potential in small volume
  - reduces chance of memory error from high temperature
- **Low power consumption** - low programming voltages and low current
  - ~300X lower power than conventional non-volatile memory
  - could increase battery life of devices
- **Low cost, scalable fabrication** - no lithography; architecture is amenable to large scale manufacturing

Publications

- Lee, S., Sohn, J., Jiang, Z., Chen, H. Y., & Wong, H. S. P. (2015). Metal oxide-resistive memory using graphene-edge electrodes. *Nature communications*, 6.

Patents

- Published Application: 20180082840
- Issued: 10,672,604 (USA)

Innovators

- H.-S. Philip Wong
- Seunghyun Lee
- Joon Sohn

Licensing Contact

Jon Gortat

Licensing & Strategic Alliances Director for Physical Science

Email